

ADS8422EVM

This user's guide describes the characteristics, operation, and use of the ADS8422 16-bit, 4-MHz parallel interface analog-to-digital converter evaluation module. A complete circuit description and a schematic diagram are included.

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1 EVM Overview

1.1 Features

- Full-featured evaluation module (EVM) for the high-speed ADS8422 16-bit, 4-MSPS, single-channel, parallel-interface, SAR-type analog-to-digital converters.
- Onboard signal-conditioning options
- Onboard reference options
- Input and output digital buffers
- Onboard decoding for stacking multiple EVMs.

2 Introduction

The ADS8422 is a 16-bit, 4-MSPS analog-to-digital converter (ADC) with an internal 4.096-V reference and a pseudo-bipolar, fully differential input. The device is a capacitor-based successive approximation register (SAR) converter with an inherent sample-and-hold. The ADS8422 has a 16-bit and an 8-bit parallel interface bus options, allowing a variety of processors to interface easily.

The ADS8422EVM is an evaluation and demonstration platform for the ADS8422 ADC. The board is a modular, flexible design which allows users to create custom analog signal-conditioning circuits, and choose reference sources and interface modes.

3 Analog Interface

The analog-to-digital converter accepts a pseudo-bipolar differential input. A pseudo-bipolar differential signal is a fully differential signal that has a common-mode voltage such that the voltage on each pin is always equal to or above zero volts. See the data sheet for specific details on recommended input voltages and common-mode range.

The positive leg of the input signal can be applied at connector P1 pin 2 (shown in [Table 1](#)) or via center pin of SMA connector J1. Likewise, the negative input signal can be applied at P1 pin1 or via center pin of SMA connector J2.

Table 1. Analog Input Connector

Description	Signal Name	Connector Pin		Signal Name	Description
Inverting Input Channel	–	P1.1	P1.2	+	Non-inverting Input Channel
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Reserved	N/A	P1.9	P1.10	N/A	Reserved
Reserved	N/A	P1.11	P1.12	N/A	Reserved
Pin tied to Ground	AGND	P1.13	P1.14	N/A	Reserved
Pin tied to Ground	AGND	P1.15	P1.16	N/A	Reserved
ADC generate common mode voltage	COMMOUT	P1.17	P1.18	N/A	Reserved
Pin tied to Ground	AGND	P1.19	P1.20	REF+	External Reference Input

3.1 Analog Input Circuitry

The analog input circuitry, consisting of three operational amplifiers, allow the user to install passive components to configure it for positive or negative gains, as well as input range scaling, filtering, and level translation (e.g., adding a DC offset). The installed operational amplifiers are housed in an industry standard SOIC footprint. This enables the user to test the converter using a wide assortment of dual- and

single-supply amplifiers housed in an SOIC package. When choosing the driver amplifier, the user should consider whether the amplifier can settle the input to a 16-bit level (0.00152%) within the sample time of the converter. The amplifier's total harmonic distortion (THD) characteristics should be better than the ADS8422 in the bandwidth of interest. Lastly, the noise generated by the amplifier needs to be as low as possible, so as not to degrade the performance of the ADS8422.

The RC circuit, at the input of the ADC, filters the input signal and helps charge the ADC sample and hold. The ADS8422EVM ships from the factory installed for a continuous low-frequency input signal with a 12- Ω and 1-nF RC circuit. The 6- Ω series resistors work with the capacitor to filter the input signal. It also isolates the amplifier from the capacitive load. The capacitor acts like a charge reservoir and provides a discharge path to for high-frequency noise and the input current transients which occur when the device switches from hold to sample mode.

In multiplexing applications, when a full-scale step is applied, the value of this RC filter must decrease. As with the driving amplifier, the RC circuit also must be able to settle the signal to a 16-bit level within the sample time. To achieve a 16-bit settling, the Tau of the RC circuit must be at least 12 or 12 RC. For example, when sampling at 4 MSPS, the sampling time is 70 ns; 12 Tau (12 \times RC) needs to be less than 70 ns. For a full-scale step input, the 6- Ω and 1-nF capacitor must be replaced with 12 Ω and 220 pF.

The negative supplies to the input amplifiers are selectable with solder jumper pad SJP1 and SJP2. Shorting across pads 1 and 2 grounds the negative rail. Shorting across pads 2 and 3 ties the negative supply of the amplifiers to the voltage applied at node -VCC.

When deciding on supply rails for bipolar amplifiers, a good rule is to add at least 2 V of headroom on either side to achieve optimal performance. For example, if the signal applied to the amplifier is 0 V – 4 V, then the amplifier rails should be at least –2 V and +6 V. Without this headroom, the amplifier-introduced distortion can become significant and degrade system performance. For CMOS or single-supply amplifiers, this is not always possible. Single-supply amplifiers distort the signal with larger amplitudes and at higher frequencies. The user may need to test the amplifier separately to understand its characteristics across the user-input conditions before using it to drive the ADS8422.

The ADS8422EVM ships with SJP1 and SJP2 pads shorted across 2 and 3.

3.1.1 Commout Pin

The ADS8422 IC generates a 2.048-V, common-mode voltage at pin 3. This voltage can be wired to the input circuit by shorting W7 between pins 1 and 2. If other voltages are necessary, set W7 pins 2 and 3 and use amplifier U5B. The ADS8422EVM ships from the factory with W7 set to pin 2 and 3.

3.2 Input Circuit

The factory-set configuration of the input driving circuitry is for a bipolar differential input signal. The necessary DC component to offset the signal at U7 and U8 is generated by U5. U5 is the low-noise THS4032 amplifier. U5 also can be configured to further filter the reference chip (U2) and provide positive gains.

[Table 2](#) indicates how the solder pad jumpers should be set to select from the various supply and input options for the analog driver circuitry.

The ADS8422EVM leaves the factory with potentiometer, R16, set to 2.048 V. The 2.048-V DC offset can be changed to 4.096 V, if the user's source is unable to DC offset the signal (see [Figure 1](#)). If a fully differential signal source is available, it is recommended that the circuit similar to [Figure 1](#) be used. For best performance, the driver amplifiers should be independent of each and set up as simple buffers. If the user's signal generator is able to provide a unipolar signal with a common mode of 2.048 V, then R14 and R11 may be removed and the input signal levels halved.

The schematic pages for the ADS8422EVM are at the end of this document. If the user can find a clean single-ended source, the ADS8422EVM's input circuitry can be reconfigured as shown in [Figure 2](#). Although not available to test on this evaluation module, for continuous signals a single THS4131 amplifier also can be used to drive the ADS8422. As mentioned earlier, the analog input circuitry is flexible and allows the user to test many different circuit configurations. If a particular circuit configuration is not possible, the user may wire in a custom driver circuit at SMA connectors J5 and J6. If bypassing the onboard circuits, be sure to remove resistors R37 and R38. For more application circuits, see the ADS8422 product data sheet.

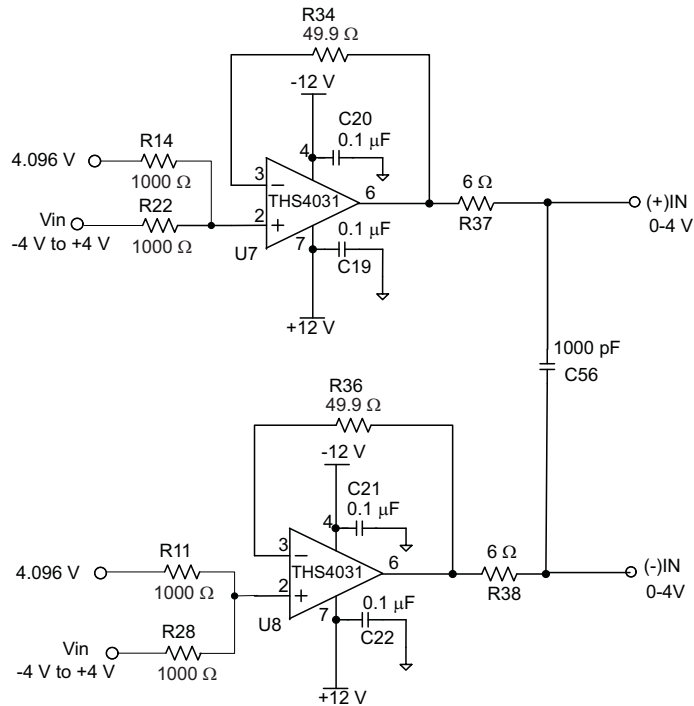


Figure 1. Bipolar Fully Differential Input

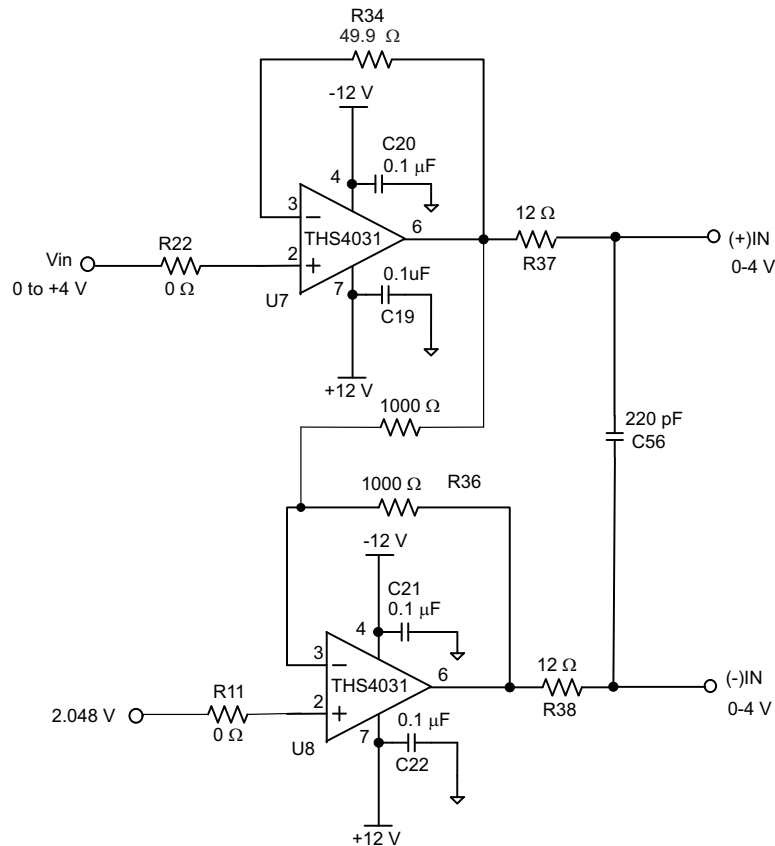


Figure 2. Unipolar Input

Table 2. Analog Circuit Jumper Configurations

Jumper	Description	Pads 1 and 2	Pads 2 and 3
SLJP1	Set U7 amplifier minus rail supply to ground	Shorted	Open
	Set U7 amplifier minus rail supply to -VCC	Open	Shorted ⁽¹⁾
SLJP2	Set U6 amplifier minus rail supply to ground	Shorted	Open
	Set U6 amplifier minus rail supply to -VCC	Open	Shorted ⁽¹⁾
SJP3	Set REFIN pin of ADS8422 to on-chip (internal) reference voltage	Shorted ⁽¹⁾	Open
	Set REFIN pin of ADS8422 to reference selected by SJP7.	Open	Shorted
SJP7	Set SJP3 pin 3 to reference IC, U1	Shorted ⁽¹⁾	Open
	Set SJP3 pin 3 to voltage at P1 pin 20.	Open	Shorted

⁽¹⁾ Indicates factory installed option.

3.3 Reference

The ADS8422 can operate with an external reference voltage in a range up to 4.15 V. This analog-to-digital converter generates an on-chip 4.096-V reference voltage and has an onboard reference buffer. The internal reference of the converter is buffered out of the device. Likewise, the external reference voltage in (on REFIN pin) is buffered inside the device, relieving the user from having to provide an external amplifier to drive the reference pin. This onboard reference buffer recharges all of the capacitors of the CDAC during conversion.

Digital Interface

The user can select the reference voltage from any one of three sources. The first option is to use the internally generated 4.096 V from the ADS8422. The other two options are to select from the onboard reference (U1) or a user-supplied voltage applied at pin 20 of P1. See [Table 2](#) for solder jumper options for selecting from the various reference sources.

The reference voltage provides the scale factor for the conversion result. The input voltage sampled is measured against the reference voltage. It is imperative the reference voltage be clean, low noise, and well decoupled.

The ADS8422EVM is shipped from the factory to use the internal on-chip reference.

Table 3. Reference Circuit Jumper Configurations

Jumper	Description	Pads 1 and 2	Pads 2 and 3
SLJP3	Set REFIN pin of ADS8422 to on-chip (internal) reference voltage.	Shorted ⁽¹⁾	Open
	Set REFIN pin of ADS8422 to reference selected by SJP7.	Open	Shorted
SLJP7	Set SJP3 pin 3 to reference IC, U1	Shorted ⁽¹⁾	Open
	Set SJP3 pin 3 to voltage at P1 pin 20.	Open	Shorted

⁽¹⁾ Indicates factory-installed option.

4 Digital Interface

The ADS8422EVM is designed for easy interfacing to multiple platforms. The digital interface input and output signals of the converter are on connectors P2, P3, J4, and J7. These are 0.1-inch-center plug and socket connectors, allowing the user to plug the ADS8422EVM onto the various motherboards and interface cards from Texas Instruments, or to use ribbon cable for the user's custom development board. The following tables list the connector pinouts.

Table 4. Pinout for Parallel Control Connector, P3

Description	Signal Name	Connector Pin		Signal Name	Description
Daughtercard chip select	$\overline{DC_CS}$	P3.1	P3.2	GND	Ground
Reserved	N/A	P3.3	P3.4	GND	Ground
Reserved	N/A	P3.5	P3.6	GND	Ground
Address line 0	A0	P3.7	P3.8	GND	Ground
Address line 1	A1	P3.9	P3.10	GND	Ground
Address line 2	A2	P3.11	P3.12	GND	Ground
Reserved	N/A	P3.13	P3.14	GND	Ground
Reserved	N/A	P3.15	P3.6	GND	Ground
Convert Start	$\overline{DC_CONVST}$	P3.17	P3.8	GND	Ground
Interrupt pin	INTC	P3.19	P3.20	GND	Ground

Conversions are initiated on the falling edge of the Convert Start signal. It is therefore critical when measuring large amplitude and/or high-frequency input signals that the user provide a clean, low-jitter Convert Start pulse.

The Convert Start signal can be applied to the ADS8422 from the decoder outputs or from connector P3 pin 17. The address decoder (SN74ACH138) is used to generate the Read (\overline{RD}), Reset, and Convert Start (\overline{CONVST}) signals to the converter. Jumpers W3, W4, and W8 allow the user to assign these signals to different addresses in memory. This allows for the stacking of up to two ADS8422EVMs into a processor's memory space. See [Table 3](#) for jumper settings. If you apply a Convert Start signal directly on P3 pin 17, then be sure to short W6 pins 1-2. This bypasses the decoder output selected by position of W4. Likewise, if you decide to drive the control signals directly at J4, be sure to remove jumpers W3, W5, W6, and W8.

Note, the evaluation module does not allow Chip Select (\overline{CS}) line of the converter to be assigned to different memory locations. It is therefore suggested that the \overline{CS} line be grounded or wired to an appropriate signal of the processor.

Table 5. Jumper Settings

Reference Designator	Description	Pads 1 and 2	Pads 2 and 3
W2	Apply inverted BUSY to INTC signal	Installed ⁽¹⁾	Not installed
	Apply BUSY signal to INTC signal	Not installed	Installed
W3	Set \overline{RD} signal to add[0x3]	Installed	Not installed
	Set \overline{RD} signal to add[0x4]	Not installed	Installed
W4	Set \overline{CONVST} signal to add[0x1]	Installed	Not installed
	Set \overline{CONVST} signal to add[0x2]	Not installed	Installed
W5	Set $\overline{DC_CS}$ to \overline{CS} of ADS8422	Installed	N/A
W6	Set $\overline{DC_CONVST}$ to \overline{CONVST} of ADS8422	Installed	Installed
	Set decoder output to \overline{CONVST} of ADS8422	Not installed	Installed
W8	Set Reset signal to add[0x5]	Installed	Not installed
	Set Reset signal to add[0x6]	Not installed	Installed

⁽¹⁾ Indicates factory-installed option.

The data bus is available at connector P2 and at J7.

Table 6. Data Bus Connector, P2

Description	Signal Name	Connector Pin		Signal Name	Description
Data Bit 0	DB0	P2.1	P2.2	GND	Ground
Data Bit 1	DB1	P2.3	P2.4	GND	Ground
Data Bit 2	DB2	P2.5	P2.6	GND	Ground
Data Bit 3	DB3	P2.7	P2.8	GND	Ground
Data Bit 4	DB4	P2.9	P2.10	GND	Ground
Data Bit 5	DB5	P2.11	P2.12	GND	Ground
Data Bit 6	DB6	P2.13	P2.14	GND	Ground
Data Bit 7	DB7	P2.15	P2.16	GND	Ground
Data Bit 8	DB8	P2.17	P2.18	GND	Ground
Data Bit 9	DB9	P2.19	P2.20	GND	Ground
Data Bit 10	DB10	P2.21	P2.22	GND	Ground
Data Bit 11	DB11	P2.23	P2.24	GND	Ground
Data Bit 12	DB12	P2.25	P2.26	GND	Ground
Data Bit 13	DB13	P2.27	P2.28	GND	Ground
Data Bit 14	DB14	P2.29	P2.30	GND	Ground
Data Bit 15	DB15	P2.31	P2.32	GND	Ground

Connector J7 can be used to plug the ADS8422EVM to the TSW1100 data capture card.

Table 7. TSW1100 Bus Connector, J7

Description	Signal	Connector Pin		Signal	Description
Ground	Ground	P7.1	P7.2	N/C	Not Connected
Ground	Ground	P7.3	P7.4	N/C	Not Connected
Ground	Ground	P7.5	P7.6	D0	Buffered Data Bit 0 (LSB)
Ground	Ground	P7.7	P7.8	D1	Buffered Data Bit 1
Ground	Ground	P7.9	P7.10	D2	Buffered Data Bit 2
Ground	Ground	P7.11	P7.12	D3	Buffered Data Bit 3
Ground	Ground	P7.13	P7.14	D4	Buffered Data Bit 4
Ground	Ground	P7.15	P7.16	D5	Buffered Data Bit 5
Ground	Ground	P7.17	P7.18	D6	Buffered Data Bit 6
Ground	Ground	P7.19	P7.20	D7	Buffered Data Bit 7
Ground	Ground	P7.21	P7.22	D8	Buffered Data Bit 8
Ground	Ground	P7.23	P7.24	D9	Buffered Data Bit 9
Ground	Ground	P7.25	P7.26	D10	Buffered Data Bit 10
Ground	Ground	P7.27	P7.28	D11	Buffered Data Bit 11
Ground	Ground	P7.29	P7.30	D12	Buffered Data Bit 12
Ground	Ground	P7.31	P7.32	D13	Buffered Data Bit 13
Ground	Ground	P7.33	P7.34	D14	Buffered Data Bit 14
Ground	Ground	P7.35	P7.36	D15	Buffered Data BIT 15
Ground	Ground	P7.37	P7.38	N/C	Not Connected
Ground	Ground	P7.39	P7.40	INT _c	Trigger Clock

This evaluation module provides direct access to all the analog-to-digital converter input control and output signals via connector J4, see [Table 8](#) for its pinout.

Table 8. Pinout for Converter Control Connector, J4

Description	Signal Name	Connector Pin		Signal Name	Description
Chip Select Signal	\overline{CS}	J4.1	J4.2	GND	Ground
Read Signal	\overline{RD}	J4.3	J4.4	GND	Ground
Convert Start Signal	\overline{CONVST}	J4.5	J4.6	GND	Ground
Byte Signal	BYTE	J4.7	J4.8	GND	Ground
Reset/Powerdown 1	$\overline{RESET/PD1}$	J4.9	J4.10	GND	Ground
Powerdown 2	$\overline{PD2}$	J4.11	J4.12	GND	Ground
Busy Signal	BUSY	J4.13	J4.14	GND	Ground

5 Power Supplies

The EVM requires four power supplies.

- A dual \pm VA DC supply for the dual-supply operational amplifiers. Recommend \pm 12-VDC supply.
- A single +5-VDC supply for analog section of the board (A/D + Reference).
- A single +5-VDC or +3.3-VDC supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1. Wire in voltages at test points on the EVM. See the following tables.

Table 9. Power Supply Test Points

Test	Point Signal	Description
T6	+BVDD	Apply +3.3 VDC or +5 VDC. See ADC data sheet for full range.
TP4	+AVCC	Apply +5 VDC.
TP3	+VA	Apply +12 VDC. Positive supply for amplifier.
TP5	-VA	Apply -12 VDC. Negative supply for amplifier.

2. Use the power connector J3, and derive the voltages elsewhere. The pinout for the connector follows. See [Table 11](#) for power supply jumper settings

Table 10. Power Connector Pinout, J3

Signal	Power Connector – J1		Signal
+VA (+12 V)	1	2	-VA (-12 V)
+5VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
+3.3VD	9	10	+5VD

Table 11. Power Supply Jumpers

Reference Designator	Description	Pads 1 and 2	Pads 2 and 3
W1	Set pin 1 of W10 supply voltage to +3.3V	Installed ⁽¹⁾	Not installed
	Set pin 1 of W10 supply voltage to +5V	Not installed	Installed
W9	Short +3.3V to board I/O supply	Installed ⁽¹⁾	Not installed
	Short +5V to board I/O supply	Not installed	Installed
W10	Short pin 2 of W1 to ADS8422 I/O supply	Installed ⁽¹⁾	Not installed
	Short voltage applied at TP14 to ADS8422 I/O supply	Not installed	Installed
W11	Short +3.0V to VAREG pin of ADS8422	Installed ⁽¹⁾	Not installed
	Short +5V to VAREG pin of ADS8422	Not installed	Installed

⁽¹⁾ Indicates factory-installed option.

6 Using the ADS8422EVM

The ADS8422EVM serves the functions of being a reference design, a prototyping board, and as a software test platform.

6.1 Reference Board

As a reference design, the ADS8422EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The layout and the bill of materials for this reference design is given in Appendixes B and C, respectively. The ADS8422EVM analog input circuit is optimized for a wide bandwidth signal; therefore, the user may adjust the input buffer circuitry to better suit the application. In applications where signal distortion is a major concern, the user should use only high-quality capacitors in the signal path such as Mica, polyester, polypropylene or COG type capacitors in the signal path. In applications where the input is multiplexed, the A/D input resistor and capacitor may need to be adjusted further. The digital buffers and special analog circuits may not be necessary in your application, but are installed on the ADS8422EVM because it is also a prototype board.

6.1.1 Development Board

As a prototype board, the ADS8422EVM features amplifiers in a standard 8-pin SOIC package and many resistor and capacitor pads are scattered around allowing the user to create and experiment with circuits, as needed. The ADS8422EVM can be used to evaluate both dual- and single-supply amplifiers in both inverting and noninverting configurations. The ADS8422EVM comes installed with a dual-supply amplifier which allows the user to take advantage of the full input voltage range of the converter. For applications that require single-supply operation and smaller input voltage range, the THS4031 can be replaced with high-speed, single-supply amplifiers like the OPA300, OPA350, etc. Be aware that pad jumper SJP1 and SJP2 should be shorted between pads 1 and 2 in this case. Doing so shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied at test point TP4 or at connector J5 pin 1.

6.1.2 Evaluation Board

Users can evaluate the ADS8422EVM's performance by two common methods.

1. EVM used as a stand-alone system. The user is responsible for capturing and analyzing the data, typically via a logic analyzer and analysis software (LABView, MATLAB, etc)
2. EVM used with TI's TSW1100 data capture card, <http://focus.ti.com/docs/toolsw/folders/print/tsw1100.html>

Method two is discussed in the following section.

6.1.3 EVM and TSW1100 Capture Card

The user's guide for the data capture card is available at <http://focus.ti.com/lit/ug/slau155a/slau155a.pdf>. See this guide for detailed information and setup instructions.

The ADS8422EVM mates with the TSW1100 card via J1, as shown in [Figure 3](#). Two data ports are available on the capture card; the reference designators are J1 and J2. [Figure B-4](#) shows how to plug the ADS8422EVM into the TSW1100 card.

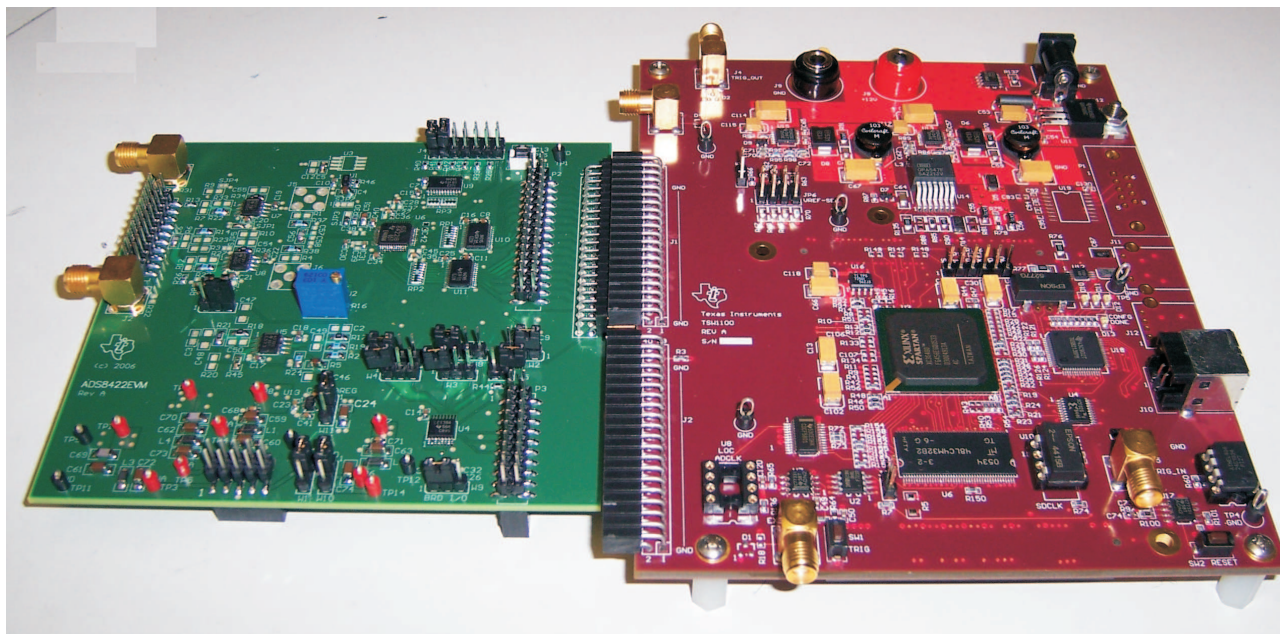


Figure 3. TSW1100 and ADS8422EVM

The TSW1100 is a data capture card and provides no control signals to the ADS8422. The ADS8422 requires a $\overline{\text{CONVST}}$ pulse to begin digitizing the signal. Therefore, the user must provide a $\overline{\text{CONVST}}$ to the ADS8422 at P3 pin 17 or at J4 pin 5 on the ADS8422EVM. In this case, it is recommended that the ADS8422 be operated in the CS and RD tied low mode, as this requires only $\overline{\text{CONVST}}$ to toggle. To short this signal to ground, simply short across pins 1 and 2 and 3 and 4 of J4, respectively. The digitized data is available on the data bus at the end of every busy cycle. In this operating scheme, the inverted BUSY signal is used to trigger the TSW1100 card to read the data bus. To avoid line contention issues, remove jumpers from W3, W4, W5, W6, and W8 on the ADS8422EVM.

The ADS8422 EVM is supported with the TSW1100 capture card firmware release 1.X. To acquire the latest TSW1100 software, send an e-mail to dataconvapps@list.ti.com.

6.2 Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5-6K Interface Board. The 5-6K Interface Board sits on the C5000™ and C6000™ digital signal processor starter kits (DSK). The ADS8422EVM then is mapped into the processor's memory space. The 5-6k Interface Board also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8422 analog-to-digital converter. For more information, see the 5-6K Interface Board user's guide ([SLAU104](#)). For example programs and instruction on how to interface this ADS8422EVM to the C5000™ and C6000™ DSKs, see the application report *ADS8422 Example Programs* ([SLAA326](#)) on the TI Web site.

For the software engineer, the ADS8422EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user need only provide three address lines (A2, A1, and A0) and address valid line ($\overline{\text{DC_CS}}$) to connector P3. To select which address combinations generate $\overline{\text{RD}}$, RESET, and $\overline{\text{CONVST}}$, set jumpers as shown in Table 5. If address decoding is not required, the EVM provides buffered access to converter data bus at P2 and control at J4.

7 Related Documentation from Texas Instruments

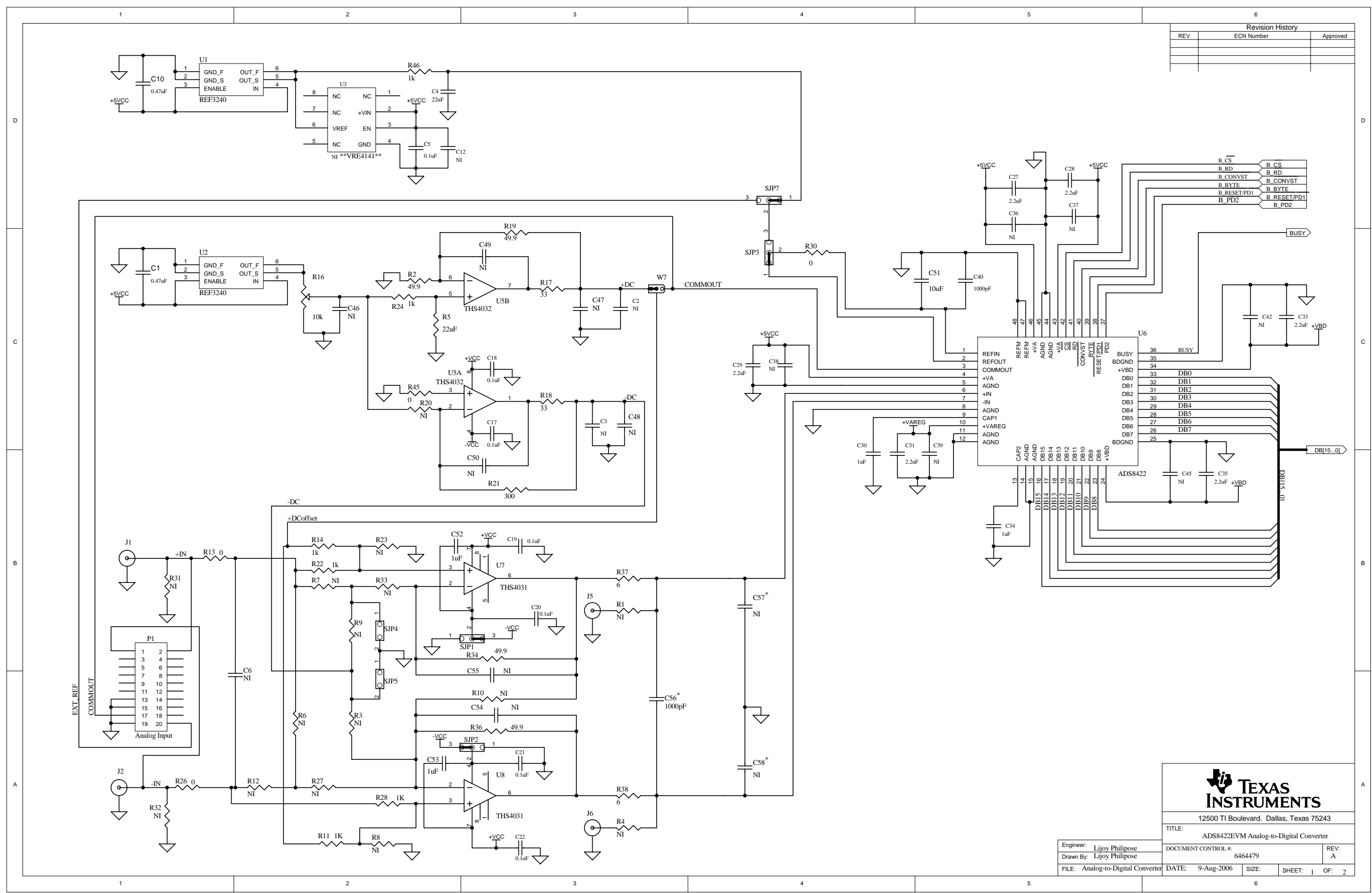
To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at <http://www.ti.com>.

Data Sheets:	Literature Number:
ADS8422	SLAS512
REF3240	SBVS058
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318
THS4031	SLOS224
THS4032	SLOS224

Appendix A ADS8422EVM Schematic

The ADS8422EVM schematic appears on the following page.

Revision History		
REV	ECN Number	Approved

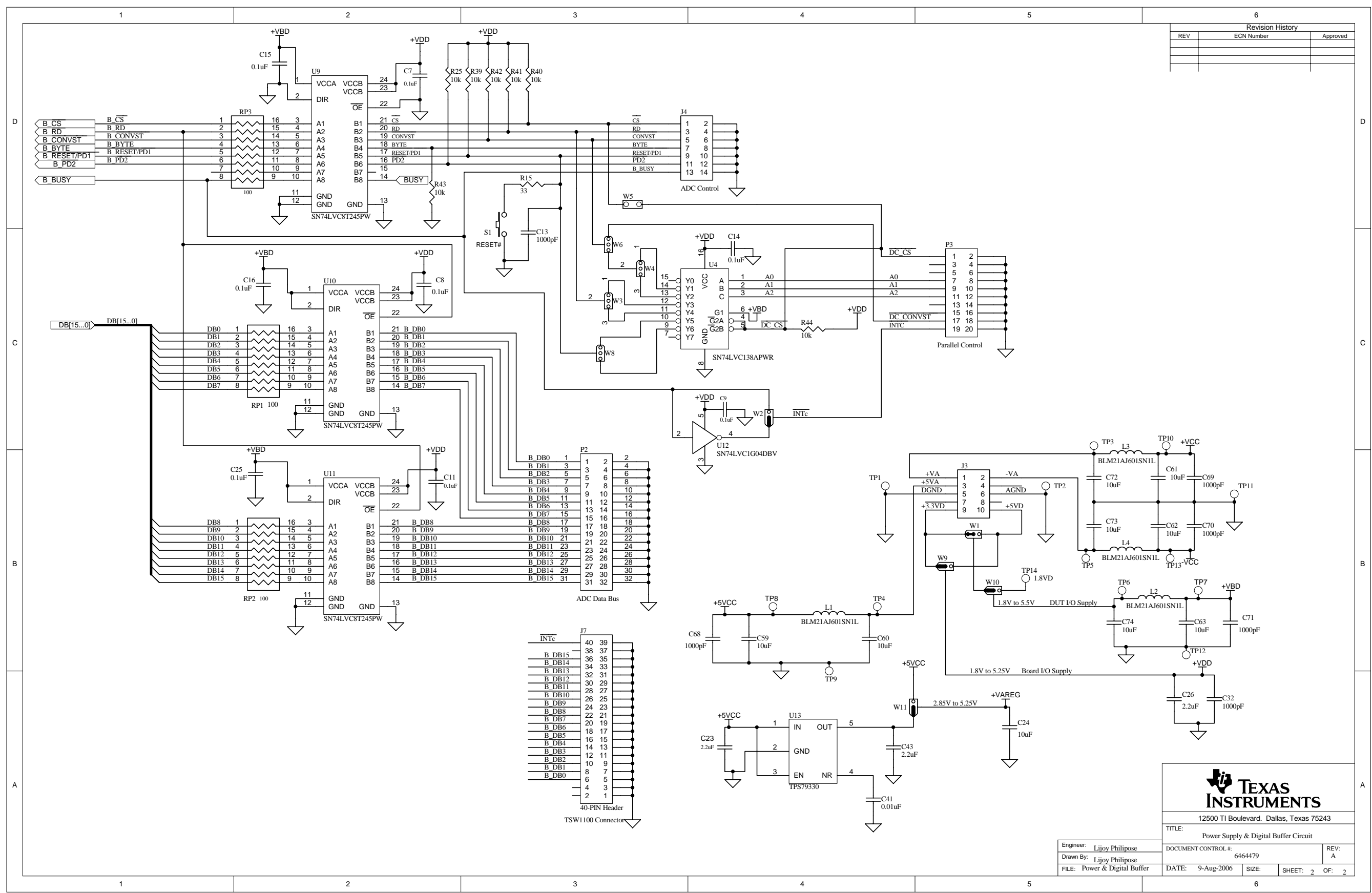


12500 TI Boulevard, Dallas, Texas 75243

TITLE: ADS8422EVM Analog-to-Digital Converter

Engineer: Lijoy Philipose	DOCUMENT CONTROL #: 6464479	REV: A
Drawn By: Lijoy Philipose	DATE: 9-Aug-2006	SIZE: SHEET: 1 OF: 2
FILE: Analog-to-Digital Converter		

Revision History		
REV	ECN Number	Approved



12500 TI Boulevard, Dallas, Texas 75243

TITLE: Power Supply & Digital Buffer Circuit
 DOCUMENT CONTROL #: 6464479
 DATE: 9-Aug-2006
 SIZE: SHEET: 2 OF: 2

Engineer: Lijoy Philipose
 Drawn By: Lijoy Philipose
 FILE: Power & Digital Buffer

REV: A

Appendix B ADS8422EVM Layout

This section presents the layout for the ADS8422EVM.

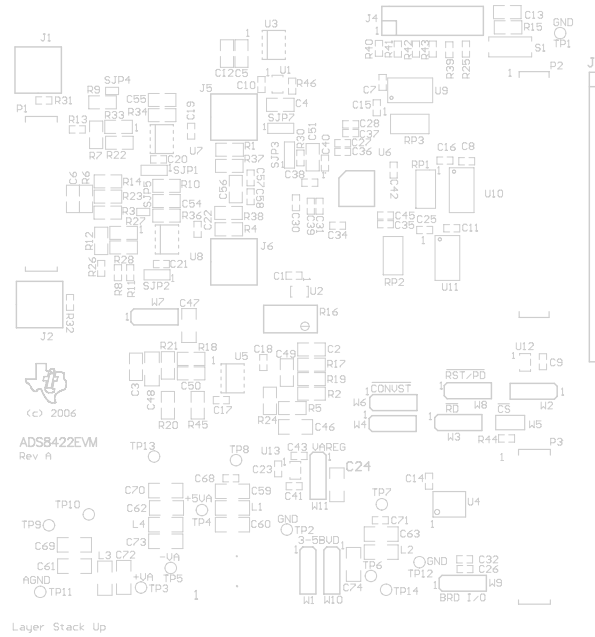


Figure B-1. Top Overlay

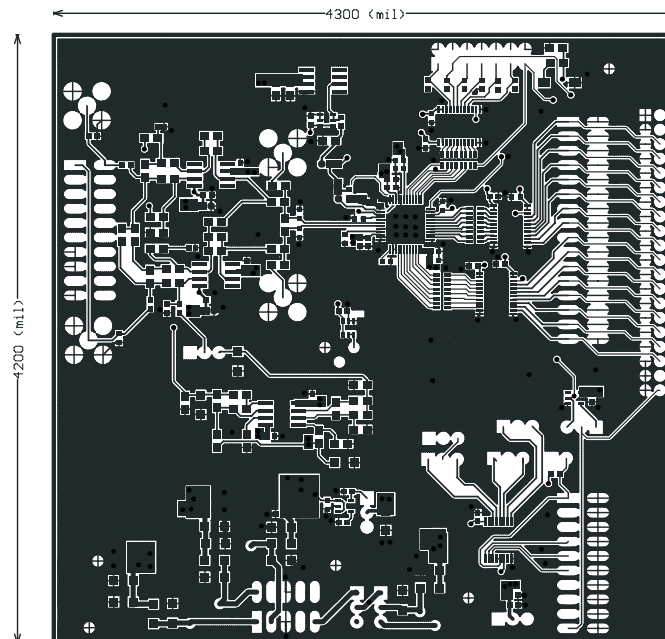


Figure B-2. Top Layer

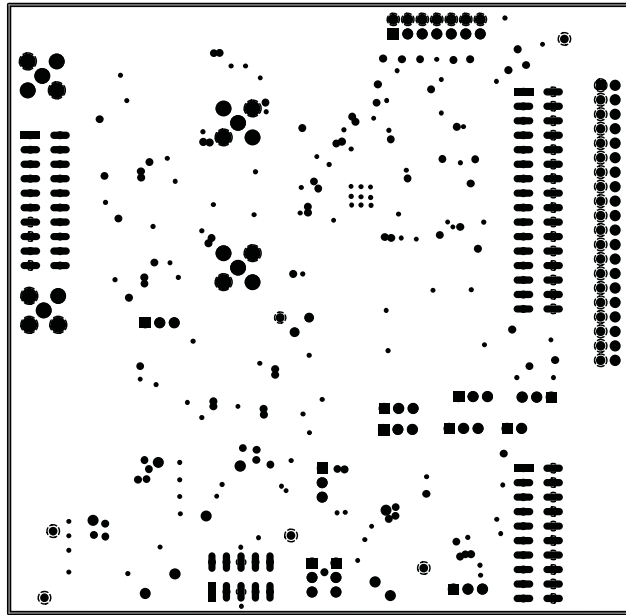


Figure B-3. Layer 2 – Ground Plane

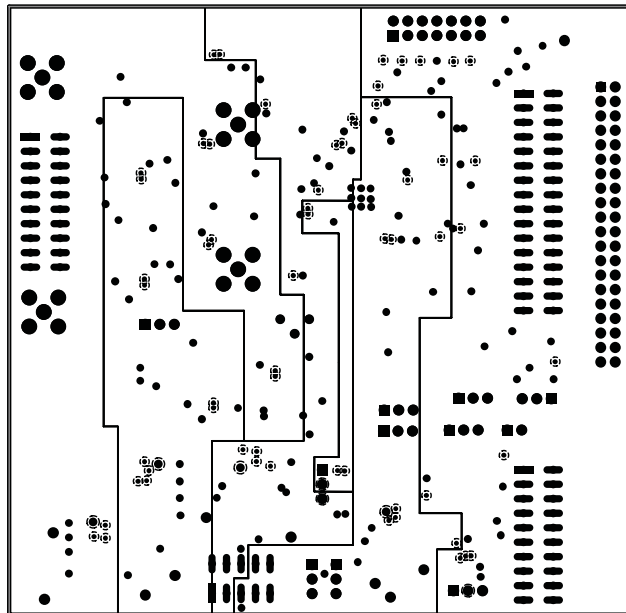


Figure B-4. Layer 3 – Power Plane

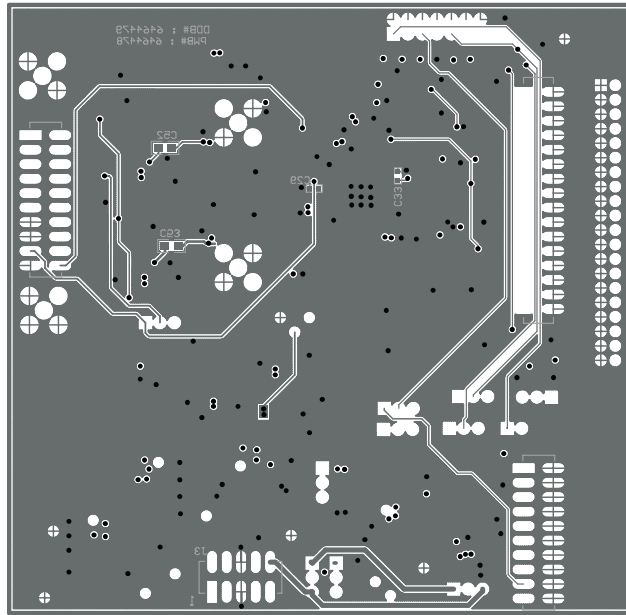


Figure B-5. Bottom Layer

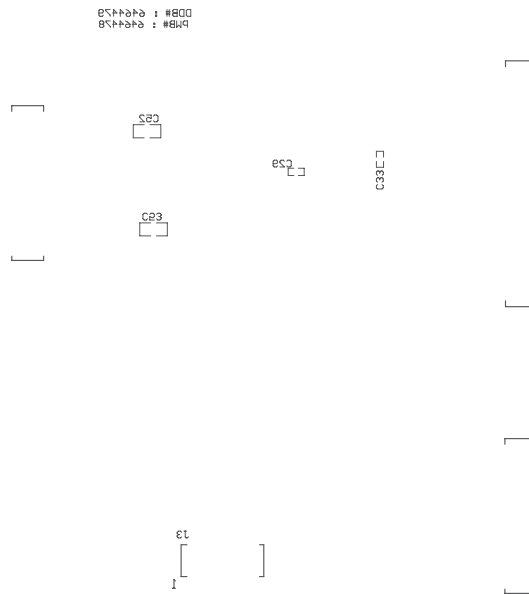


Figure B-6. Bottom Over Lay

Appendix C ADS8422EVM Bill of Materials

This appendix provides the ADS8422EVM bill of materials. Contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

Qty.	Value	Reference Designators	Footprint	Mfg.	Mfg's Part No.	Description
12	NI	R1 R33 R3 R4 R6 R7 R9 R10 R12 R20 R23 R27	805	Not Installed	Not Installed	1/10W 0805 Chip Resistor
3	NI	R8 R31 R32	603	Not Installed	Not Installed	1/10W 0603 Chip Resistor
3	0	R13 R26 R30	603	Panasonic – ECG or Alternate	ERJ-3GEY0R00V	RES 0Ω 1/16W 5% 0603 SMD
1	0	R45	805	Panasonic - ECG or Alternate	ERJ-6GEY0R00V	RES 0.0Ω 1/10W 5% 0805 SMD
2	6	R37 R38	805	Yageo America or Alternate	9C08052A6R04FG HFT	RES 6.04Ω 1/8W 1% 0805 SMD
3	33	R15 R17 R18	805	Panasonic - ECG or Alternate	ERJ-6GEYJ330V	RES 33Ω1/8W 5% 0805 SMD
4	49.9	R2 R19 R34 R36	805	Panasonic - ECG or Alternate	ERJ-6ENF49R9V	RES 49.9Ω 1/8W 1% 0805 SMD
3	100	RP1 RP2 RP3	CTS_742	CTS Corporation	742C163101JTR	RES ARRAY 100Ω 16TRM 8RES SMD
1	300	R21	805	Yageo America or Alternate	9C08052A3000FK HFT	RES 300Ω 1/8W 1% 0805 SMD
2	1K	R11 R46	603	Panasonic - ECG	ERA-3YEB102V	RES 1.0kΩ 1/16W .1% 0603 SMD
4	1K	R14 R22 R24 R28	805	Panasonic - ECG	ERA-6YEB102V	RES 1.0kΩ 1/10W .1% 0805 SMD
7	10k	R25 R39 R40 R41 R42 R43 R44	603	Panasonic - ECG or Alternate	ERJ-3KEF1002V	RES 10.0kΩ 1/10W 1% 0603 SMD
1	10k	R16	BOURNS_32 96Y	Bourns Inc.	3296Y-1-103	POT 10kΩ 3/8" SQ CERM SL MT
4		L1 L2 L3 L4	1206	TDK Corporation	MMZ2012R601A	Ferrite chip 600Ω 500mA 0805
9	NI	C6 C36 C37 C38 C39 C42 C45 C57 C58	603	Not Installed	Not Installed	
7	NI	C2 C3 C12 C49 C50 C54 C55	805	Not Installed	Not Installed	
3	NI	C46 C47 C48	1206	Not Installed	Not Installed	
4	1000pF	C32 C40 C68 C71	603	TDK Corporation or Alternate	C1608X7R1H102K	CAP CER 1000pF 50V XR7 10% 0603
2	1000pF	C13 C56	805	TDK Corporation or Alternate	C2012C0G1H102J /10	CAP CER 1000pF 50V C0G 0805 T/R

Appendix C

Qty.	Value	Reference Designators	Footprint	Mfg.	Mfg's Part No.	Description
2	1000pF	C69 C70	1206	TDK Corporation or Alternate	C3216C0G2J102J	CAP CER 1000pF 630V C0G 5% 1206
1	0.01μF	C41	603	TDK Corporation or Alternate	C1608X7R1H103KT	CAP CER 10000pF 50V X7R 10% 0603
15	0.1μF	C5 C7 C8 C9 C11 C14 C15 C16 C17 C18 C19 C20 C21 C22 C25	603	TDK Corporation or Alternate	C1608X7R1E104K	CAP CER 0.10μF 25V X7R 10% 0603
2	0.47μF	C1 C10	603	TDK Corporation or Alternate	C1608X5R1A474K	CAP CER 0.47μF 10V X5R 10% 0603
2	1μF	C30 C34	603	TDK Corporation or Alternate	C1608X5R1A105KT	CAP CER 1.0μF 10V X5R 10% 0603
2	1μF	C52 C53	805	TDK Corporation or Alternate	C2012X7R1E105K	CAP CER 1.0μF 25V X7R 0805 T/R
9	2.2μF	C23 C26 C27 C28 C29 C31 C33 C35 C43	603	TDK Corporation or Alternate	C1608X5R1A225MT	CAP CER 2.2μF 6.3V X5R 20% 0603
1	10μF	C51	805	TDK Corporation or Alternate	C2012X5R0J106M	CAP CER 10μF 6.3V X5R 20% 0805
9	10μF	C24 C59 C60 C61 C62 C63 C72 C73 C74	1206	TDK Corporation or Alternate	C3216X5R1C106M	CAP CER 10μF 16V X5R 20% 1206
2	22μF	C4 R5	805	TDK Corporation or Alternate	C2012X5R0J226M	CAP CER 22μF 6.3V X5R 20% 0805
2		U1 U2	6-SOT(DBV)	Texas Instruments	REF3240AIDBVR	Low drift reference REF 3225, 3230, 3233, 3240
1	NI	U3	8-SOP(D)	Not Installed	Not Installed	VRE4141 4.096V high precision bandgap reference that operates from +5V.
1		U4	16-TSSOP(PW)	Texas Instruments	SN74LVC138APWR	3-8 Line DEC/DEMUL
1		U5	8-SOP(D)	Texas Instruments	THS4032CD	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
1		U6	48-TQFP(PFB)	Texas Instruments	ADS8422IBPFBT	16-Bit 4MSPS ADC
2		U7	U8 8-SOP(D)	Texas Instruments	THS4031IDR	100-MHz Low-noise high-speed amplifier
3		U9 U10 U11	24-TSSOP(PW)	Texas Instruments	SN74LVC8T245PW	8-bit dual supply bus transceiver with voltage translation and 3-state outputs
1		U12	5-SOT(DBV)	Texas Instruments	SN74LVC1G04DBV	Single Inverter
1		U13	5-SOT(DBV)	Texas Instruments	TPS79330DBVR	Ultralow-noise, high PSRR, Fast RF 200-mA Low-dropout linear
2		J1 J2	SMA_JACK	Johnson Components Inc.	142-0701-301	Right Angle SMA Connector
1	5X2X.1	J3	5X2X.1_SMT_SOCKET	Samtec	SSW-105-22-S-D-VS	0.025" SMT Socket - bottom side of PWB
1				Samtec	TSM-105-01-T-D-V-P	0.025" SMT Plug - top side of PWB

Qty.	Value	Reference Designators	Footprint	Mfg.	Mfg's Part No.	Description
1	7X2X.1	J4	7X2X.1	Samtec	TSW-107-11-T-D	7 Pin Dual Row Header
2	NI	J5 J6	SMA_JACK	Not Installed	Not Installed	MaCom #5002-5003-10 / Amphenol #901-144
1	40-Pin Header	J7	20X2X.1	Samtec	TSW-120-11-T-D-RA	Right Angle 40 pin connector
2	10X2X.1	P1 P3	10X2X.1_SMT_PLUG_SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT socket – bottom side of PWB
2				Samtec	TSM-110-01-T-D-V-P	0.025" SMT Plug - top side of PWB
1			16X2X.1_SMT_PLUG_SOCKET	Samtec	SSW-116-22-S-D-VS	0.025" SMT socket – bottom side of PWB
1				Samtec	TSM-116-01-T-D-V-P	0.025" SMT plug - top side of PWB
2		SJP4 SJP5	SJP2	Not Installed	Not Installed	
4		SJP1 SJP2 SJP3 SJP7	SJP3	Not Installed	Not Installed	
1		S1	EVQ-PJ	Panasonic	EVQ-PJU04K	Switch
1		W5	2pos_jump	Samtec	TSW-102-07-L-S	2 Position Jumper _ .1" spacing
10		W1 W2 W3 W4 W6 W7 W8 W9 W10 W11	3pos_jump	Samtec	TSW-103-07-L-S	3 Position Jumper _ .1" spacing
9		TP3 TP4 TP5 TP6 TP7 TP8 TP10 TP13 TP14	test_point2	Keystone Electronics	5000K-ND	Test point PC MINI 0.040" D Red
5		TP1 TP2 TP11 TP12 TP9	test_point2	Keystone Electronics	5001K-ND	Test point PC MINI 0.040"D Black

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